AMENDMENTS TO THE CLAIMS

1. (original) A method of forming a field-effect transistor, comprising:
forming a channel region within a bulk semiconductor material of a semiconductor substrate, wherein the channel region comprises a first monocrystalline material;
exposing a portion of the first monocrystalline material to a surface of the semiconductor substrate;
performing an epitaxial deposition upon the exposed portion of the first monocrystalline material, thereby forming extensions of second monocrystalline material; and
forming source/drain regions on opposing sides of the channel region, wherein the source/drain regions are in contact with the extensions of second monocrystalline material.

2. (original) The method of claim 1, wherein the first monocrystalline material is a doped monocrystalline silicon material.

3. (original) The method of claim 2, wherein the second monocrystalline material is a doped monocrystalline silicon material.

4. (original) The method of claim 2, wherein the second monocrystalline material is a silicon-germanium alloy.

5. (original) The method of claim 4, wherein the silicon-germanium alloy comprises between approximately 20-50 at% germanium.

6. (original) The method of claim 1, wherein performing an epitaxial deposition further comprises performing an epitaxial deposition in the presence of a dopant material.

7. (original) The method of claim 6, wherein the dopant material is a conductivity enhancing material.

8. (original) The method of claim 6, wherein the dopant material is germanium.

9. (original) The method of claim 1, wherein forming source/drain regions further comprises forming source/drain regions of a polycrystalline material.

10. (original) The method of claim 9, wherein the polycrystalline material is polycrystalline silicon.

11. (original) The method of claim 10, wherein the polycrystalline silicon is doped to have a conductivity type opposite of a conductivity type of the bulk semiconductor substrate.

12. (currently amended) A method of forming a field-effect transistor, comprising:
forming extensions of monocrystalline material ~~interposed between source/drain regions of the field-effect transistor and~~ extending away from a channel region of the field-effect transistor.

13. (original) The method of claim 12, wherein forming extensions of monocrystalline material further comprises forming extensions of epitaxial silicon.

14. (original) The method of claim 13, wherein forming extensions of epitaxial silicon further comprises forming extensions of doped epitaxial silicon.

15. (original) The method of claim 14, wherein the doped epitaxial silicon is doped with germanium.

16. (original) The method of claim 12, wherein forming extensions of monocrystalline material further comprises forming extensions of epitaxially grown silicon-germanium alloy.

17. (original) The method of claim 16, wherein the silicon-germanium alloy comprises approximately 20 at% germanium or more.

18. (original) The method of claim 17, wherein the silicon-germanium alloy further comprises no more than approximately 50 at% germanium.

19. (currently amended) A method of forming a field-effect transistor, comprising:
forming extensions of monocrystalline silicon interposed between a polycrystalline portion of silicon source/drain regions of the field-effect transistor and a monocrystalline silicon channel region of the field-effect transistor.

20. (original) The method of claim 19, wherein forming extensions of monocrystalline silicon further comprises performing an epitaxial silicon deposition.

21. (original) The method of claim 20, wherein performing an epitaxial silicon deposition further comprises performing an epitaxial silicon deposition in the presence of a dopant gas.

22. (currently amended) A method of forming a field-effect transistor, comprising:
forming extensions of silicon-germanium alloy interposed between a polycrystalline portion of silicon source/drain regions of the field-effect transistor and a monocrystalline silicon channel region of the field-effect transistor.

23. (original) The method of claim 22, wherein forming extensions of silicon-germanium alloy further comprises performing an epitaxial growth of the silicon-germanium alloy.

24. (currently amended) A method of forming a field-effect transistor, comprising:
performing an epitaxial silicon growth subsequent to forming a channel region of the field-effect transistor and prior to forming source/drain regions of the field-effect transistor;
wherein the epitaxial silicon is grown on exposed portions of monocrystalline silicon to form the epitaxial silicon ~~interposed between~~ extending away from the channel region ~~and the source/drain regions~~.

25. (currently amended) A method of forming a field-effect transistor, comprising:
performing an epitaxial growth of silicon-germanium alloy subsequent to forming a channel region of the field-effect transistor and prior to forming source/drain regions of the field-effect transistor;
wherein the epitaxial growth of silicon-germanium alloy is grown on exposed portions of monocrystalline silicon to form the silicon-germanium alloy ~~interposed between~~ extending away from the channel region ~~and the source/drain regions~~.

26. (original) A method of forming a field-effect transistor, comprising:
forming a region of monocrystalline silicon to define a channel region;
exposing a portion of the region of monocrystalline silicon;
growing epitaxial monocrystalline silicon from the exposed portion of the region of monocrystalline silicon; and
forming a region of polycrystalline silicon in contact with the epitaxial monocrystalline silicon to define a source/drain region.

27. (original) A method of forming a field-effect transistor, comprising:
forming a region of monocrystalline silicon to define a channel region;

exposing a portion of the region of monocrystalline silicon;

growing epitaxial silicon-germanium alloy from the exposed portion of the region of monocrystalline silicon; and

forming a region of polycrystalline silicon in contact with the epitaxial silicon-germanium alloy to define a source/drain region.

28. (original) A method of forming a field-effect transistor, comprising:

forming a first trench in a bulk semiconductor substrate on a first side of a channel region within the bulk semiconductor substrate;

forming a second trench in the bulk semiconductor substrate on a second side of the channel region within the bulk semiconductor substrate;

forming a layer of dielectric material within each trench;

removing a portion of the layer of dielectric material to define a first source/drain void in the first trench and a second source/drain void in the second trench and to expose a portion of the bulk semiconductor substrate in each source/drain void;

forming extensions of monocrystalline material on the exposed portions of the bulk semiconductor substrate in each source/drain void;

forming source/drain semiconductive material within each source/drain void and to be in contact with the extensions of monocrystalline material; and

forming a gate over the channel region.

29. (original) The method of claim 28, wherein forming extensions of monocrystalline material on the exposed portions of the bulk semiconductor substrate in each source/drain void further comprises growing epitaxial silicon on the exposed portions of the bulk semiconductor substrate in each source/drain void.

30. (original) The method of claim 29, wherein growing epitaxial silicon further comprises growing undoped epitaxial silicon.

31. (original) The method of claim 28, wherein forming extensions of monocrystalline material on the exposed portions of the bulk semiconductor substrate in each source/drain void further comprises growing epitaxial silicon-germanium alloy on the exposed portions of the bulk semiconductor substrate in each source/drain void.

32. (original) A method of forming a field-effect transistor, comprising:

forming a first trench in a monocrystalline silicon substrate on a first side of a channel region within the monocrystalline silicon substrate;

forming a second trench in the monocrystalline silicon substrate on a second side of the channel region within the monocrystalline silicon substrate;

forming a layer of dielectric material within each trench;

removing a portion of the layer of dielectric material to define a first source/drain void in the first trench and a second source/drain void in the second trench and to expose a portion of the monocrystalline silicon substrate in each source/drain void;

forming extensions of monocrystalline silicon on the exposed portions of the monocrystalline silicon substrate in each source/drain void; and

forming polycrystalline silicon within each source/drain void and to be in contact with the extensions of monocrystalline silicon; and

forming a gate over the channel region.

(claims 33-59 cancelled)